

# Identifying Component Parasitics Using Equivalent Circuit Modelling

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Within circuit simulations, only the ideal case is considered. This is insufficient in many ways as it is not possible for a physical component to act ideal outside of a very limited frequency range. In order to account for this equivalent circuit modelling can be applied to identify the parasitic elements introduced by a components imperfections and structure. There are two broad methods which can be applied to obtain an equivalent circuit model. The first is a heuristic approach, which is a brute force form of guess and check in which an approximated topology and values is applied. However, this method is not suitable for high complexity analysis. The second method explored uses partial fraction expansion to separate a transfer function of the input frequency response into a series of fractions. These fractions can then be compared to known circuit topology equations such that an equivalent circuit model can be produced. In doing this there remains a degree of experimentation for the input variables being the number of poles and zeros of the function, determining the order, as well considering both the impedance and admittance of the input frequency response. The use of the PFE method allows for a simplified analysis, compared to that of the heuristic approach. The PFE also produces a higher degree of accuracy when considering the magnitude of either the impedance or the admittance, with the extent of this dependent upon the accuracy used in determining a sufficient equivalent model when using the heuristic approach. In each case, the modelling method produces an equivalent circuit topology, which has an output more closely resembling that of a measured input than the ideal response. This can then be used for the purpose of circuit simulations, allowing for a higher degree of accuracy within the production of component and circuit behaviour.

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## Nomenclature

Terms:

RLC Resistor Inductor Capacitor circuit

PFE Partial Fraction Expansion

Variables

$f$  = frequency [Hz]

$\omega$  =  $2\pi f$

$C$  = Capacitor [F]

$L$  = Inductor [H]

$R$  = Resistor [ $\Omega$ ]

$j$  =  $\sqrt{-1}$

$s$  = s Domain (Laplace domain)

$Y(s)$  &  $Z(s)$  = Admittance and impedance in s domain

$Y(\omega)$  &  $Z(\omega)$  = Admittance and impedance in frequency domain

## I. Introduction

Within the design and development of electrical circuits an accurate and thorough understanding of each of the components used is essential to ensure accurate function. This is because components will only function ideally within a specific frequency range. Currently the majority of simulation capabilities only simulate the ideal case for any given component. While these simulations provide a level of information anything outside of or nearing the components ideal operating range will be effected by parasitics.

Within the physical construction of components the imperfections within the materials used as well as the construction result in behaviour which does not comply with the ideal model. These behaviours represent the parasitics of each component. Within the analysis of RLC components these parasitics can be characterised by an R, L or C component or a combination of components.

For the identification of equivalent circuit topologies to represent the parasitics present there are two broad methods, the first of these is the Heuristic approach. Heuristics represents a brute force type approach and attempts to match a topology through analysis of the frequency response data. The heuristic approach relies heavily upon a thorough understanding of RLC circuits and their given frequency response outputs. Due to this, the method becomes highly complex particularly for responses which require complex topologies and hence is not easily applicable to the analysis of complex circuits. In order to achieve more accurate equivalent circuit models a more complex analysis can be conducted. Within this project, the focus for this analysis was the use of PFE for the production of the equivalent topologies. This method also relies on an approximate transfer function fitting and accurate analysis of the PFE output through a comparison with known circuit topology equations. The PFE method also required a level of experimentation, however it represents a process for equivalent circuit modelling which has a higher accuracy and reduced uncertainty.

In both cases the resultant equivalent circuit topologies are only representative of the frequency response of the input across the given range of the data. This is because the behaviour of the frequency response outside of this. In addition, due to the nature of physical measurements, a fully accurate fit is not possible outside of fabricated data. As such, any topology that is developed from an output frequency response is only an estimation for the given input.

## II. Heuristics

The main consideration within the Heuristic approach undertaken is that of the data at the extremes as well as at any peak or trough. The heuristic example given is that of a 1000pF capacitor. Through analysis of the magnitude of the impedance, it can be seen that the frequency response has passed through the resonant frequency, this being represented by the trough depicted in Figure 1.

As a result if the frequency range passing through resonance, the response at higher frequencies is more influenced by the parasitics of the component than that of the ideal response.

To determine the resistance of the circuit, the trough of the plot is used. If a resistance was not present, the trough would occur at a magnitude of  $0\Omega$ , instead it occurs at the resistance value  $R=0.62\Omega$ . For the remaining elements, ideal topology equations are considered. These being:

For a series configuration:

$$\text{Inductor} = j\omega L \quad (1)$$

$$\text{Capacitor} = \frac{1}{j\omega C} \quad (2)$$

And for parallel:

$$\text{Capacitor} = j\omega C \quad (3)$$

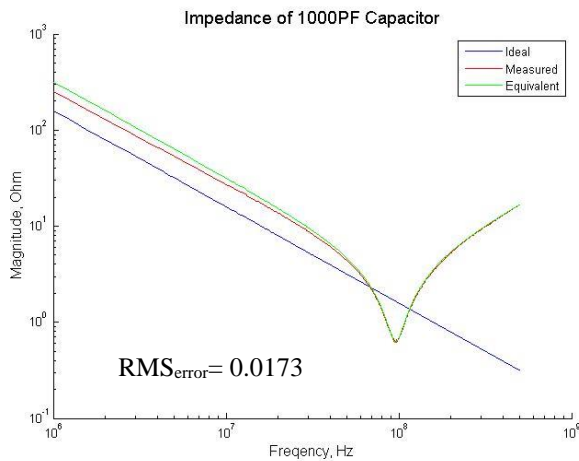
$$\text{Inductor} = \frac{1}{j\omega L} \quad (4)$$

From this the configuration for the given data is likely a series RLC. Where the capacitance,  $\frac{1}{j\omega C}$  is the greatest influence at low frequencies while as frequency increases the influence tends more to  $j\omega L$ . This being represented by Equation 1 and Equation 2. From this the likely topology is a series RLC configuration.

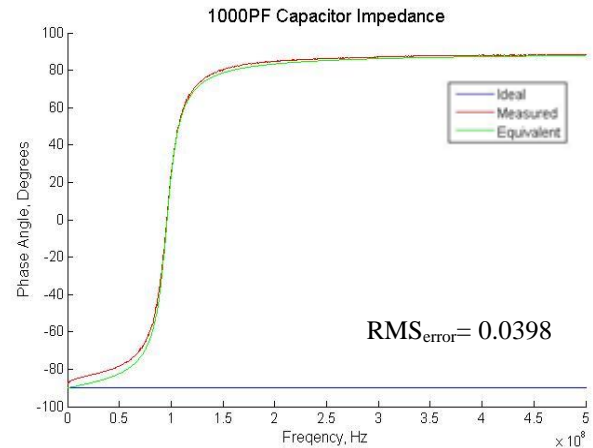
Through the manipulation of this data the values for each of the components can be determined. This was achieved by considering the imaginary component of the data at the extremes this being as frequency tends to zero and infinity. The imaginary data is used due to the influence of the  $j$  term within the specifications of both the inductance and the capacitance. Multiplication and division were then used to obtain the component values. Within this, the average value over a small range at the extremes was taken, this was done as there was identifiable variation within the regions of interest.

This analysis produced an output of,  $C = 499 \text{ pF}$  and  $L = 5.5 \mu\text{H}$ . as can be seen from this the value determined for the capacitance is not close to that of the input value. Through a comparison of the input data to the equivalent model, an RMS error of 0.0173 for the magnitude and 0.0398 for the phase angle which was

calculated using  $RMS_{error} = \sqrt{\frac{1}{N} \sum_{k=1}^N |H_{Model}(k) - H_{Input}(k)|^2}$ . From this comparison, it can be seen that the produced model is a good fit to the input data over the given frequency range. The results of the Magnitude and phase angle comparisons are shown in Figure 1 and figure 2 respectively.



**Figure 1. Magnitude of Impedance – ideal, measured and equivalent circuit comparison**



**Figure 2. Phase Angle of Impedance – ideal, measured and equivalent circuit comparison**

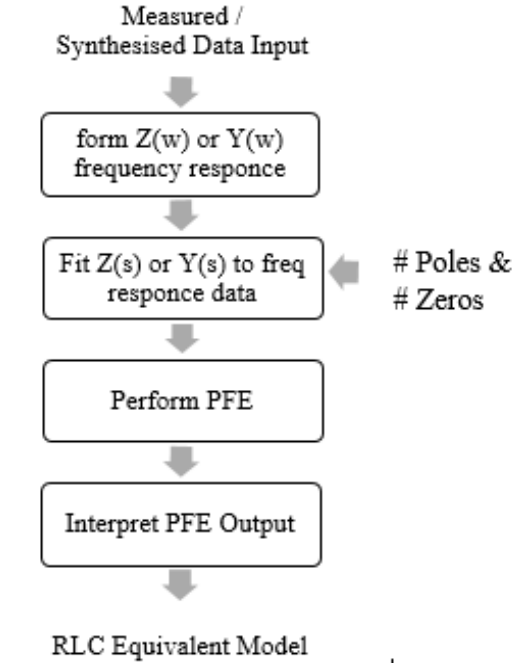
Through a comparison of the measured and equivalent outputs in Figure 1 and Figure 2, a good correlation can be seen between the data sets. This the equivalent modelling through heuristic methods can be applied effectively. However, for more complex configurations, the application of this method becomes impractical due to the level of guessing required.

### III. Equivalent Modelling Using PFE

#### A. Data management

The input data for the PFE process can take two forms, these being synthesised data or measured data. The synthesised data was used in the development and testing phases of the system. Knowing the structure of the overall process the data was developed such that it represented  $Z(\omega)$  or  $Y(\omega)$  being the impedance or admittance of the chosen topology. This was done to minimise the level of data processing required.

In the case of measured data, the reflection coefficient was taken this being the  $S_{11}$  parameter for the system. This was a convenient form for the measurement instrument used. However, the process can be modified to accommodate for other input forms. A system calibration was performed prior to the taking of any measurements.



**Figure 3. PFE Process Flow Chart**

In which  $Un1$  is the input frequency response being either the inductance or the admittance,  $wN$  is the normalised frequency range,  $z$  is the number of zeros denoting the order of the numerator and  $p$  is the number of poles denoting the power of the denominator. The remaining variables are used for the purpose of function stabilisation. From this the factors of the numerator and the denominator are produced with  $b$  denoting the numerator and  $a$  denoting the denominator.

At this stage the accuracy of the transfer function must be considered. This is primarily achieved through the visual comparison of the input frequency response to that of the produced transfer function. Initially a Heuristic approach may be applied such that an approximate number of poles and zeros for the function is determined. However, to determine the accuracy of the produced model, some additional approximation of values is required to evaluate the effect on the accuracy of the system output.

To achieve this the value of both the number of poles and number of zeros is altered individually beginning with the presumed topology. Observations are made of the effect of each change on the overall output. Within this the aim for the equivalent model is to be both accurate and simple, that is, that it is of the lowest order possible while maintaining a high level of accuracy. In order to assist with the analysis, the RMS error can be calculated such that a quantitative measure of accuracy is provided.

As a result of this step, the form of the data is transferred from the form  $H(jw)$  to  $H(s)$ . The main impact of this is that the output form the function can only represent an approximation of the data presented. The input response used is only representative of a slice within a 3D system of which only a limited frequency range is considered. Hence, the model produced can only be applied as an acceptably accurate approximation within the restrictions of the input data.

### C. Partial Fraction Expansion

The basis for using PFE to produce the equivalent topologies is that the output can be compared to known circuit topology equations. The overall function of a PFE is to expand the transfer function, determined using `invfreqs`, into a sum of simple terms. This being from the form in Equation 6 to that of Equation 7, in which each term is representative of a series of connected impedances for a  $Z(s)$  input, and admittances for a  $Y(s)$  input.

$$H(s) = \frac{D(s-\alpha_1)(s-\alpha_2)(s-\alpha_3)(s-\alpha_4)}{(s-\beta_1)(s-\beta_2)(s-\beta_3)} \quad (6)$$

$$H(s) = D + Es + \frac{F}{s-\beta_1} + \frac{G}{s-\beta_2} + \frac{H}{s-\beta_3} \quad (7)$$

$$[r, pp, k] = \text{residue}(b, a) \quad (8)$$

Within the production of the frequency responses, a normalisation of the input data with respect to  $w$  was performed. This was done to minimise any system error which results from the limitations of system accuracy. Normalisation achieves this by reducing the order of the components which are influenced by the normalising factor being  $w$ . This is achieved through a division of the  $w$  variable by the maximum value of  $w$ . In general the maximum value of  $w$  used was  $6.2832 \times 10^9$  Hz corresponding to a maximum frequency of 1 GHz. From this the value of  $w$  becomes  $wN = w/\max(w)$ . As normalisation is used, a denormalisation is also required to determine the value of components with relation to  $w$  these being the capacitor and inductor values. This is performed with the output of the PFE.

### B. Fit $Z(s)$ or $Y(s)$ to frequency Response Data

The second step within the process is the production of a transfer function which approximates a fit to a given function order. This was achieved through the application of MATLAB's `invfreqs` function. The function is applied using the form denoted in Equation 5.

$$[b, a] = \text{invfreqs}(Un1, wN, z, p, [], 30) \quad (5)$$

The PFE of the transfer function produced from the data is achieved through the use of MATLAB's residue function. This takes the outputs from invfreqs representing the numerator and denominator and provides three outputs. The first is the residue vector denoted by r, this represents the fraction numerators, pp represents the pole values while the k is any whole number outputs. There will only be a value for k if the order of the numerator is greater than that of the denominator. From the three output components the overall form of the PFE can be represented by Equation 9 where n and m are representative of whole numbers.

$$H(s) = k(1)s^{n-1} + k(2)s^{n-2} + \dots + k(n) + \frac{r(1)}{s - pp(1)} + \frac{r(2)}{s - pp(2)} + \dots + \frac{r(m)}{s - pp(m)} \quad (9)$$

This output is then analysed. Firstly it must be determined if the topology is realisable or not. This meaning that the equivalent circuit topology is physically possible. To determine this the values from k, r, and pp each have to be considered. If the circuit is to be realisable, the values for k and r must all be positive ensuring positive component value outputs, while the values for pp must be negative to ensure pole stability within the left half plane. In the case that the topology is not realisable, it will be removed as an alternative with the experimentation of possibilities to be continued.

#### D. Interpretation

**Table 1: Circuit Configurations and Resulting Impedance and Admittance Equations**

Topology	Z (s)	Poles/zeros (Z)	Y (s)	Poles/zeros (Y)
R	$R$	$z = 0$ $p = 0$	$\frac{1}{R}$	$z = 0$ $p = 0$
L	$sL$	$z = 1$ $p = 0$	$\frac{1}{sL}$	$z = 0$ $p = 1$
C	$\frac{1}{sC}$	$z = 0$ $p = 1$	$sC$	$z = 1$ $p = 0$
Series RL	$R + sL$	$z = 1$ $p = 0$	$\frac{1}{\frac{R}{L} + s}$	$z = 0$ $p = 1$
Series RC	$R + \frac{1}{sC}$	$z = 0$ $p = 1$	$\frac{s + \frac{1}{RC}}{\frac{1}{C}}$	$z = 1$ $p = 0$
Series LC	$sL + \frac{1}{sC}$	$z = 1$ $p = 2$	$\frac{s^2 + \frac{1}{LC}}{\frac{s}{C}}$	$z = 2$ $p = 1$
Parallel RL	$\frac{sR}{s + \frac{R}{L}}$	$z = 1$ $p = 1$	$\frac{1}{R} + \frac{1}{sL}$	$z = 1$ $p = 1$
Parallel RC	$\frac{\frac{1}{C}}{s + \frac{1}{RC}}$	$z = 0$ $p = 1$	$\frac{1}{R} + sC$	$z = 1$ $p = 0$
Parallel LC	$\frac{\frac{1}{C}}{s^2 + \frac{1}{LC}}$	$z = 1$ $p = 2$	$\frac{1}{sL} + sC$	$z = 2$ $p = 1$
Series RLC	$R + sL + \frac{1}{sC}$	$z = 2$ $p = 1$	$\frac{\frac{s}{L}}{s^2 + \frac{sR}{L} + \frac{1}{LC}}$	$z = 1$ $p = 2$
Parallel RLC	$\frac{\frac{s}{C}}{s^2 + \frac{s}{CR} + \frac{1}{LC}}$	$z = 1$ $p = 2$	$\frac{1}{R} + \frac{1}{sL} + sC$	$z = 2$ $p = 1$

Once an output of the PFE is determined to be realisable the equivalent circuit model can be determined. This is achieved through the comparison of the output to known circuit topologies. As the number of poles and zeros is known as well as the form of consideration for the frequency response, being the impedance or the admittance

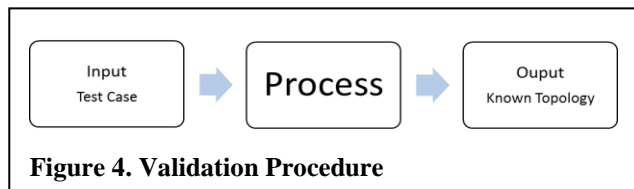
there is often only one topology to consider. However there are instances in which multiple topologies could apply. This is the case within the addition of a resistor to a simpler topology, as the influence of resistors is real only. Hence, a resistor does not influence the order of the function, this being based upon the terms with an  $s$  parameter being the inductors and capacitors. The comparison of the PFE output is made using the circuit topologies outlined in Table 1. For more complex circuits, the output components are compared to these topologies, with useable terms being identified. From this the components influence on the frequency response is then removed and the process reinitiated, allowing for the process to be repeated on the simplified response. The additional outputs are then combined with the previous output topologies to create the overall equivalent circuit.

After the output topology format has been determined the value of the components can be identified. The main aspect to be remembered at this stage is that the values produced which correspond to inductors and capacitors must be denormalised to obtain the correct values. This is done by dividing the output by the normalising coefficient being the maximum value of  $w$ .

Once the equivalent circuit configuration and component values have been determined the overall accuracy of the model must be confirmed. This is done in two ways. Firstly the plot of the equivalent circuit frequency response is to be compared to that of the input. If desired the equivalent circuit frequency response can also be compared to the intermediate outputs. If a significant discrepancy is found, the comparison to the intermediaries as well as the input may assist in identifying the issue that has occurred. The second comparison to be made is of the difference between the output frequency response and the input frequency response. For the purpose of this project the RMS error is used for this comparison and is made between the magnitude and phase frequency response data.

If the model is determined to be an accurate approximation of the input, the topology can then be used for simulation purposes.

#### IV. Process Validation

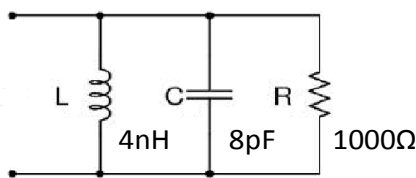


**Figure 4. Validation Procedure**

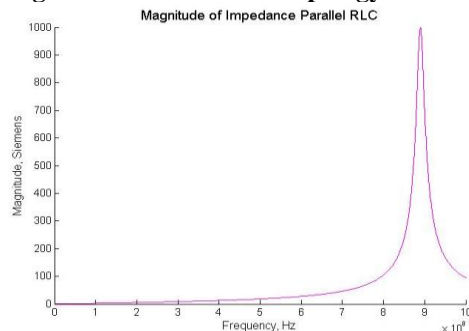
In order to validate the process, a series of known input topologies were used as test cases. This included both series and parallel configurations as well as some simple composite systems. To achieve this more easily the first three stages of the overall process, being the data initialisation, transfer function production and the

PFE were combined. This enabled the determination of realisable circuits for each variation of pole and zero combinations within the experimental range. However, the overlay of each of the output plots from these stages is still to be compared for analysis purposes.

An example of a topology used is depicted in Figure 5.



**Figure 5. RLC Parallel Topology**



**Figure 6. Magnitude of Impedance - Known Topology**

Within this example the maximum value for the frequency is 1GHZ, this resulting in a normalisation coefficient,  $w_{Max}=6.2832 \times 10^9$  Hz.

The first step in the analysis of an input is a basic heuristic approach. Considering the magnitude of the impedance as shown in Figure 6, it can be seen that there is a clear peak within the plot with the data tending to 0 at both extremes. From this the likely influence is a parallel system, based upon equations 3 and 4. As such the main focus of the analysis will be on the admittance of the frequency response. This is because the know equation for a parallel system is most comparable to a PFE output when considering the admittance, refer to Table 1,  $Y(s)$ .

Considering the admittance, experimentation of the number of poles and zeros required was then conducted. The initial order chosen was 2 zeros and 1 pole. This corresponding both the expected heuristic values as well as the known configuration. In order to verify that this was the most appropriate topology, further testing of the number of poles and zeros required was conducted.

It was found that for a number of higher order systems, the corresponding topology was not realisable. This resulting from the functions attempt to continue to fit the data. In

addition it was found that was a reduction of the system order, a level of accuracy was lost. As such, it was determined that the order of best fit was that of the known input, being 2 zeros and 1 pole for a parallel topology. For completeness, analysis was also conducted for the impedance of the frequency response input. However, the outputs were generally not realisable or were not of a form that was easily converted into an equivalent topology, these representing topologies with complex poles. From the chosen form, the output of the PFE was determine, this is shown in Equation 10.

$$Y(s) = 0.0050s + 0.0010 + \frac{0.3979}{s+2.0101e-35} \quad (10)$$

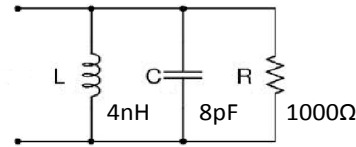
$$Y(s) = sC + \frac{1}{R} + \frac{1}{sL} \quad (11)$$

Through comparing the format of  $Y(s)$  as given by the PFE output and that of the expected topology, it can be seen that there is a correlation between the equations. It was determined that the  $2.01e-35$  is insignificant within the calculation of the inductor value and is ignored. This value results from the inherent form of the function used to produce the required output.

$$R = \frac{1}{0.0010} \quad R = 1000\Omega$$

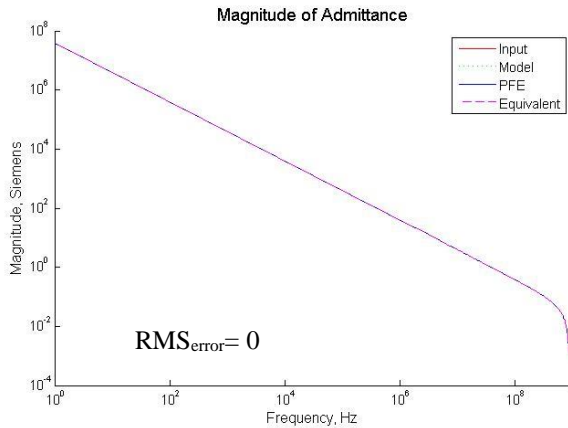
$$L = \frac{1}{0.3979 \omega_{Max}} \quad L = 4nH \text{ and}$$

$$C = \frac{0.0050}{\omega_{Max}} \quad C = 8pF.$$

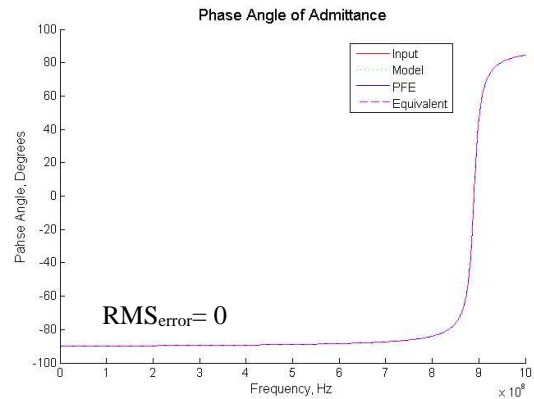


**Figure 7. Equivalent Circuit Topology**

In each instance the input component value was obtained through the interpretation of the PFE output. As such, the process can be used to accurately recreate a known topology. The output at each stage of the process for the Magnitude and phase of the admittance is shown in Figure 8 and Figure 9.



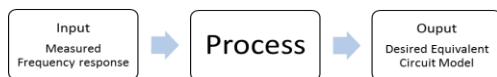
**Figure 9. Phase Angle Comparison – Input, Transfer Function, PFE and Equivalent Model**



**Figure 8. Magnitude Comparison – Input, Transfer Function, PFE and Equivalent Model**

Within the comparison of the input frequency response and the determined equivalent circuit topology, it was found that the RMS error for both the magnitude of the admittance as well as for the phase angle was 0. This showing that the equivalent circuit topology is a highly accurate representation of the input in this case. Through this and other idealized examples, it was determined that the process was working fully and as such could be applied to measured data.

## V. Measured Data Results



**Figure 10. Measured Data Analysis**

Through the application of the PFE process on measured data, equivalent models were produced. The overall accuracy of these models depends on two aspects. Firstly, and predominantly this depends on the fit of the function used for the PFE to determine the topology, as



such, the order of best fit is required to achieve a high level of accuracy. Secondly, the imperfections within the component results in complex frequency response outputs. These complexities cannot easily be modelled with a function and as such will provide a level of error between the input frequency response and the frequency response of the equivalent topology.

To provide a measure of the accuracy of the PFE process, the following example used the same input data as that of the heuristic case, being the 1000pF capacitor. For this case, the order of best fit was determined to be that of a series RLC topology. Considering the impedance with two zeros and one pole, the following PFE output was produced.

$$Z(s) = 16.8379s + 0.5908 + \frac{0.5304}{s + 2.3939e - 004} \quad (12)$$

From this the following component values were determined.

$$R = 0.59\Omega$$

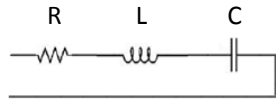
$$C = \frac{1}{0.5304}$$

$$L = \frac{wMax}{16.8379}$$

$$C = 600 \text{ pF}$$

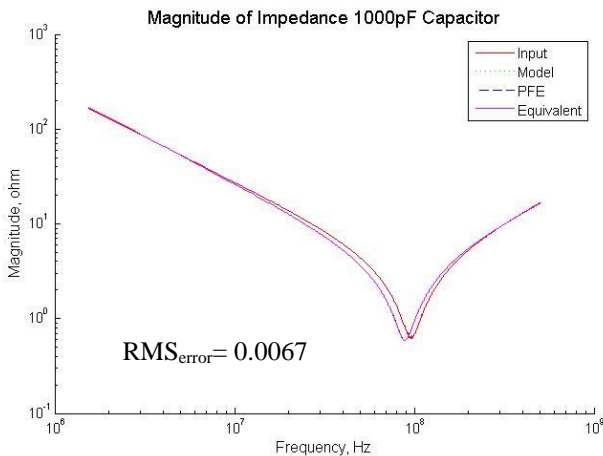
$$L = 5.36 \text{ nH.}$$

This representing the topology depicted in Figure 11.

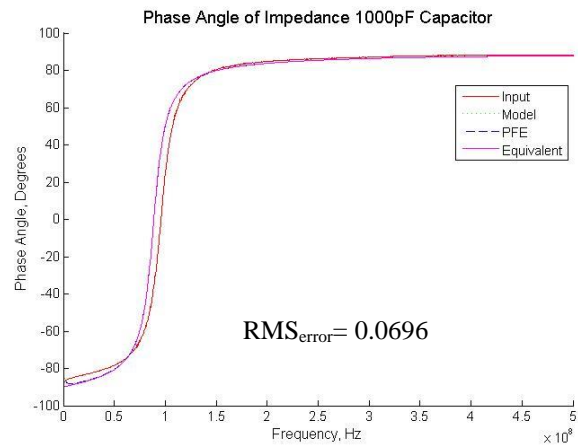


**Figure 11. Series RLC Topology**

The frequency response of the impedance for this equivalent topology was then plotted against the input frequency response as well as each of the intermediate outputs. Figure 12, depicts the Magnitude of the frequency response while Figure 13 depicts the phase angle. As can be seen there is a good correlation between the equivalent circuit topology frequency response and that of the input.



**Figure 12. Magnitude of Impedance - Comparison Equivalent Model to Input**

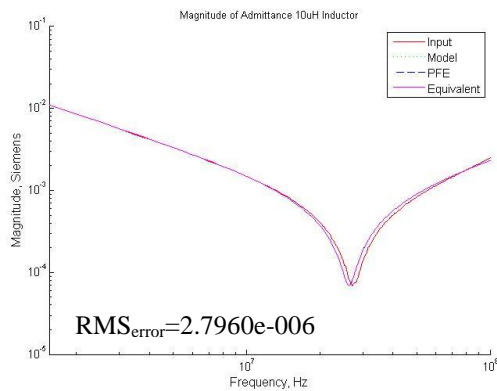


**Figure 13. Phase angle of Impedance - Comparison Equivalent Model to Input**

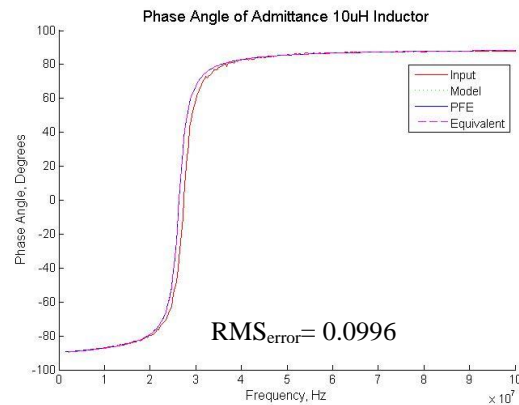
From the results for the RMS error as depicted in figure 12 and 13, the equivalent model does represent a good correlation to the input. In the case of the magnitude of impedance, the average error of the output is less than one percent, while for the phase angle this error is approximately 7%. Considering the heuristic results that were obtained from the same data the PFE process has produced a more accurate model with regards to the Magnitude of impedance with an improvement in RMS error of 1.06%. The RMS error for the phase angle has increased for the case of the PFE process. This is not as expected, however, within the heuristic approach there is a high reliance on human decision in which case the error of the phase angle was likely to be given a higher priority. In both cases presented an equivalent model of high accuracy was produced, showing the effect of both functions. However, it is clear that through the application of the PFE process a significantly reduced effort is required to produce the given output.



The second example given for measure data is for that of a 10uH inductor. Within this analysis it was determined that the order of best fit would be a two poles one zero system when considering the impedance. This is as expected from a heuristic understanding of the input. Although this is the expected case, experimentation was conducted for both the admittance and impedance with a range of pole and zero values.



**Figure 14. Magnitude of Admittance of 10uH inductor**



**Figure 15. Phase Angle of Admittance 10uH inductor**

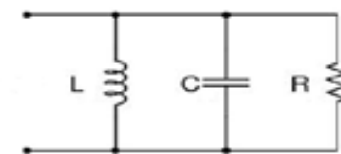
The resulting outputs are shown in figure 14 and figure 15. The determination of the equivalent circuit component values resulted in the following topology:

$$Y(s) = 0.0025s + 0.0001 + \frac{1.7228e-004}{s + 9.1361e-005} \quad (13)$$

$$R = \frac{1}{0.0001} \quad R = 14\,280\Omega$$

$$L = \frac{1}{\frac{1.7228e-004}{w_{Max}}} \quad L = 9.2162\mu\text{H and}$$

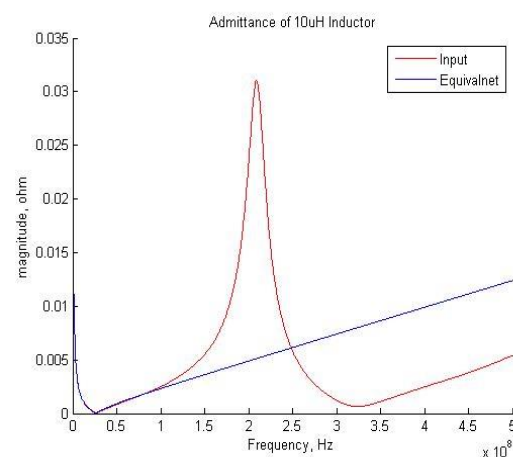
$$C = \frac{0.0025}{w_{Max}} \quad C = 3.95\text{pF}$$



**Figure 16. Equivalent Circuit Topology**

From the comparison of the equivalent topology frequency response data to that of the input, there is a good level of correlation within the results. Additionally, the value obtained from the inductor is close to that of the component expected value of 10uH. As previously found, the accuracy of the magnitude plot is better than that of the phase, however, the level of accuracy remains within reason for the application of the equivalent circuit topology.

However, as for any equivalent model, the determined topology is only accurate across the frequency range for which it was formed. For the 10uH inductor, additional data was measured over an increased frequency range, incorporating additional resonant frequencies. The Magnitude plot depicted in Figure 17 is a comparison of the model determined above with the additional data of the 10uH inductor, impedance frequency response. Outside of the range used to calculate the equivalent model being up to 1GHz, there is a good correlation between the input data and that of the Equivalent model. However, outside of this range there is significant error between the impedance of the equivalent circuit topology and the impedance of the measured data. Thus emphasizing the restriction which results from the input frequency range.



**Figure 17. Admittance of 10uH inductor - extended frequency response**

As such, when constructing the equivalent models it is important to consider the frequency range over which data acquisition will occur. Within determining the frequency range two points should be considered, firstly the frequency range over which the component or circuit will be used and secondly the value of any resonant frequencies within this range. This ensures that the frequency range of focus is covered. If a resonant frequency point is approximately after the expected cut off, it is likely to be beneficial to extend the frequency range to include this point. Alternatively, the inclusion of multiple resonant frequencies within the chosen measurement range requires a more complex model for equivalent topology. This resulting from the transition from one major influence to the other being the capacitance or inductance of the component or circuit.

## **VI. Conclusions**

Within the development and application of each stage of the PFE for equivalent circuit modelling, it was found to be possible to produce an output that was of an acceptable fit to the input data. As such through the application of the process, it is possible to create equivalent circuit topologies for RLC components and circuits, with examples of both a measured inductor and capacitor being performed. Due to the limited scope of the ideal models, the use of equivalent circuits can be highly beneficial in the analysis of components as well as overall circuit frequency responses. However within this there are a number of aspects which need to be properly understood and applied. This includes a thorough understanding of the behaviour of RLC components to allow for the application of some heuristic analysis. This decreasing the level of experimentation required in identifying a suitable equivalent circuit topology. In addition to this, the application of any model developed should only be done so across the frequency range for which it was developed. By taking this into account and adequately experimenting with the number of poles and zeros as well as considering both the impedance and admittance frequency responses the development and application of equivalent models becomes a viable option within the field of circuit simulations. Through the use of more accurate simulations, the overall behaviour of a component or subsequent circuit can be understood to a higher degree.

## **VII. Recommendations**

The primary future expansion for this work is to apply the equivalent circuit models to the components to a simulation within a circuit. From this the circuit can be simulated and physically constructed in order to compare the results. This being the next stage of process confirmation.

In addition to this, a wider range of components and component values can be analysed such that a pattern or generalisation could be determined. This could be based upon a resonant frequencies of the components. Another aspect that could be considered within this is the expected value of the input component and its corresponding value within the PFE output. Within this, it could be explored at what stage if any does the output component value differ greatly than that expected. This should also be considered in any analysis as the component used for measurements may also be faulty.

Additionally investigation into the effect of passing a resonant frequency upon the equivalent model should be conducted. Within what has been discovered so far, this is more pertinent for the inductors however, with the limited amount of measurements taken this may not be the case. In addition to this, exploring the production of models for component which have passed multiple resonant frequencies could be explored. Although this has been examined slightly there is a wide range of possibilities within this area.

Finally the analysis of frequency responses of circuits could be conducted. The results from this could then be compared to the individual component equivalent models. What this aims to examine is the potential for component combinations to occur such that the equivalent model of the circuit may be simpler than the combined models of the components. Alternatively, a more complex system may result.

## **VIII. Acknowledgements**

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